IN THE SPECIFICATION:

Please amend the third full paragraph appearing on page 2 as follows:

In the microelectronics industry, a substrate refers to one or more semiconductor layers or structures ~~which includes~~ that include active or operable portions of semiconductor devices. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including but not limited to bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term ~~substrate~~ "substrate" refers to any supporting structure including but not limited to the semiconductive substrates described above.

Please amend the paragraph bridging pages 3 and 4 as follows:

Further processing of semiconductor structure 10, including thermal processing, causes complications that arise in the prior art. The right half of Figure 1 depicts one prior art problem. It can be seen that, due to a large stress between oxide husk 20 and interconnect 12, oxide husk 20 has delaminated from interconnect 12 due to adhesion failure, and pushed upwardly to form a void 22 immediately above interconnect 12. Void 22 causes planarity problems and can also lead to underetched trenches prior to metal fill. The delamination of oxide husk 20 is an indication of a relatively thick oxide over interconnect 12. The thickness of oxide ~~husk~~ husk 20 can range from about 10Å to about 500Å. Oxide husk 20 needs to be removed prior to deposition of a metal line. The presence of void 22 causes a prominence in the ILD topology. The prominence can lead to underetched trenches prior to metal fill, resulting in the metal line not making sufficient electrical contact with interconnect 12. In addition, the prominence caused by the formation of void 22 can be formed during ILD deposition. Additionally, the prominence formed due to void 22 could cause some imaging problems because of a departure from substantial planarity of the upper surface of the ILD.

Please amend the third full paragraph appearing on page 5 as follows:

A preferred embodiment of the present invention comprises providing a semiconductor structure including a dielectric layer. Following the formation of the

dielectric layer, a depression is formed in the dielectric layer. The depression terminates at an electrically conductive structure therebeneath. The depression is then filled with an interconnect that is composed of an electrically conductive material, such as a refractory metal, and preferably tungsten. After filling of the depression with the interconnect, an upper surface of the interconnect and dielectric layer is formed by a method such as ~~chemical-mechanical~~ chemical-mechanical planarization (CMP).

Please amend the third full paragraph appearing on page 10 (including the footnote that is part of that paragraph) as follows:

The chemical compound may be, by way of non-limiting example, the ~~nitrogen-containing~~ nitrogen-containing chemical compound such as ammonia that has been adsorbed onto upper surface 16 of interconnect 12 sufficiently to substantially chemically cover or "blind off" substantially any chemically reactive portion of upper surface 16 of interconnect 12 during formation of ILD layer 18. Use of preferred chemical compounds that are to be matched with specific materials comprising interconnect 12 can be selected by one of ordinary skill in the art using such data and equations as Langmuir's monolayer adsorption isotherm or those also taught by Brunauer, Emmett, or Teller. Of interest to selection of a particular chemical compound in connection with a preferred material for interconnect 12, will be any one of the five types of adsorption isotherms as classified by ~~Brunauer[1]~~. Brunauer.[1]

1 O. Hougen *et al.*, *Chemical Process Principles 2nd Ed.*, ~~*Chapter 10: Adsorption.*~~ Chapter 10: Adsorption. John Wiley and Sons, Inc. (1954).

Please amend the third full paragraph appearing on page 11 as follows:

According to the present invention, a first example is set forth below. Following the formation of dielectric layer 14, as illustrated in Figure 2, depression 26 such as a contact corridor is formed therein, exposing semiconductor substrate 24 that may be, by way of ~~non-limiting~~ non-limiting example, a metallization line. Following the exposure of semiconductor substrate 24, a titanium liner layer 28 or the like is formed within depression 26. Subsequently, a titanium nitride layer 30 or the like is formed upon titanium liner layer 28. Titanium nitride

layer 30 may be formed by thermal nitridation of a portion of titanium liner layer 28, by deposition of titanium nitride thereupon, or by a combination thereof.

Please amend the first full paragraph appearing on page 13 as follows:

Completion of this example is carried out by the formation of second depression 34 in ILD layer 18. Accordingly, a masking layer is patterned upon upper surface 36 of ILD layer 18 and an anisotropic etch is carried out to form second depression 34. The etch recipe is selective to interconnect 12 as well as titanium liner layer 28, titanium nitride ~~layer 32,~~ layer 30, and optionally to dielectric layer 14.

Please amend the third full paragraph appearing on page 14 as follows:

Following the formation of titanium nitride layer 30, interconnect 12 is formed by deposition of tungsten into depression 26. The deposition of tungsten into depression 26 in order to form interconnect 12 may be facilitated by the presence of titanium nitride layer 30 and titanium liner layer 28. Where the formation of interconnect 12 is formed by ~~force-filling~~ force-filling of tungsten into depression 26, the presence of titanium nitride layer 30 and titanium liner layer 28 facilitate slippage of the tungsten material along the region of what will become upper surface 16 and into depression 26 so as to fill depression 26.